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(54) Overheating detection circuit for detecting overheating of a power device.

(57) An arrangement for detecting overheating of a power integrated circuit includes a power device integrated in a semiconductor substrate (11) and an overheating detection circuit. The overheating detection circuit includes a reverse biased pn junction (13, 16) formed in the same semiconductor substrate (11) as the power device and having a reverse leakage current flow which is temperature dependent, and a voltage convertor (2) formed in the same semiconductor substrate (11) as the power device and coupled to the pn junction (13, 16) for producing a voltage proportional to the reverse leakage current flow. A threshold circuit is connected for receiving the proportional voltage and producing a signal when the proportional voltage exceeds a threshold voltage (V_{th}) to indicate that the power device is overheated.

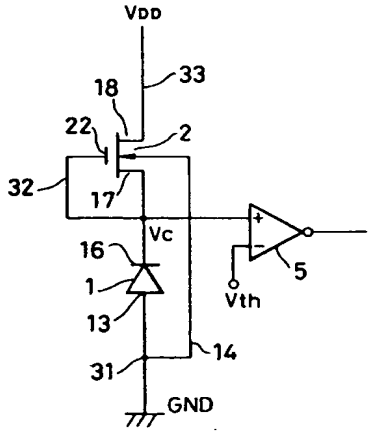
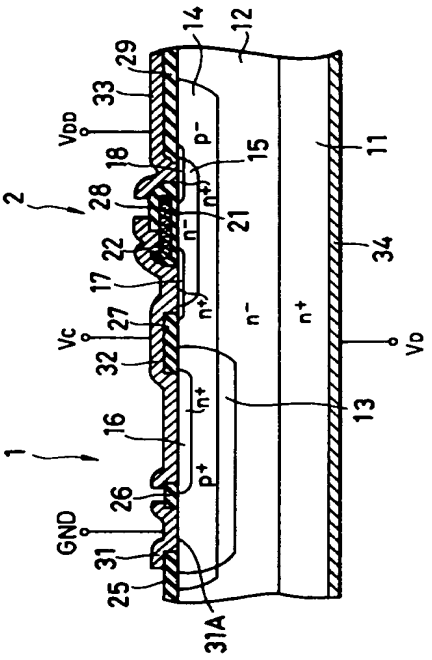


FIG.5

EP 0 488 088 A1


2
1
GND
Vc
VDD
VD
p+
p-
n+
n-
11
12
13
14
15
16
17
18
21
22
25
26
27
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29
31
31A
32
33
34

FIG.3

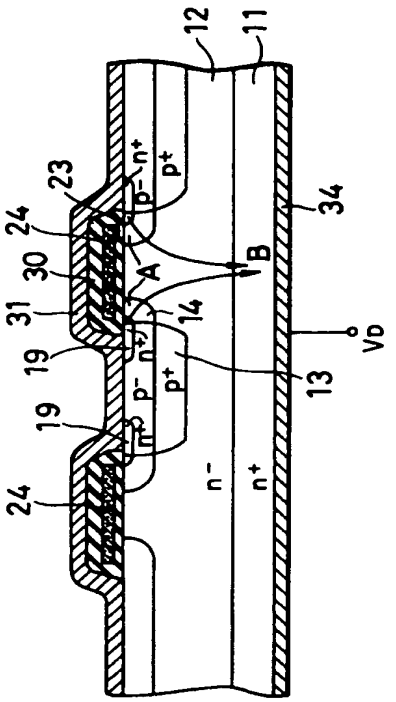

A
B
VD
p+
p-
n+
n-
11
12
13
14
19
23
24
30
31
34

FIG.4

The present invention relates to an overheating detection circuit which is formed in the same semiconductor substrate as that of a power device in a power controlling integrated circuit (power IC), and which can detect an abnormal temperature of the power device.

A power IC includes a control region having a logic region and a power device which are formed in the same substrate. Because a power IC is used with high voltages and large currents, an abrupt increase in the consumption of electric power caused by an abrupt change in a load connected to the device or a shortcircuiting of the load can result in large currents in excess of the rated current flowing through the device, thereby creating a danger that the device will become excessively heated and, in an extreme case, that the device will be destroyed. To protect a power device against such thermal destruction, the temperature of the power device is constantly monitored and, when the temperature of the device exceeds a predetermined temperature or an overheating of the device is detected, some protective action is taken, for example, the power IC is turned-off.

In monitoring a power device, it is preferable to fabricate an overheating detection circuit including a temperature sensor into a substrate in which the power device is formed in order to improve temperature sensitivity and to simplify the circuit arrangement. Typically, however, discrete elements have been used for forming a circuit which interrupts operation of a power device upon detection of eddy currents or an overheating of the power device. In this connection, a thermal sensor using a bipolar transistor as a thermo-sensitive sensor is described in E. Habekotte', Bull, ASE/UCS 76 (1985) 5, 9mars, pp. 272-276.

Fig. 1 illustrates a circuit arrangement of an overheating detection circuit of the prior art which uses the thermal sensor described in the above-cited reference. As shown in Fig. 1, a bipolar transistor 91, operating as a thermal sensor, is inserted into a feedback loop of an operational amplifier 92. An external constant current source (not shown) supplies a collector current IC to the transistor 91. Operational amplifier 92 produces an output voltage V_1, which is equal in amplitude but of reverse polarity to a base-emitter voltage V_{BE} of transistor 91. As shown in Fig. 2, the base-emitter voltage V_{BE} varies linearly with and is inversely proportional to temperature T. By properly amplifying the output voltage V_1 of the operational amplifier 92 by another operational amplifier 94, an output voltage Vout which varies linearly with respect to temperature T can be obtained.

A feature of the above thermal sensor is that the output voltage Vout varies linearly with respect to change in temperature, and that little error exists over a broad range of temperature change. However, when the thermal sensor is assembled with a power IC as an overheating detection circuit, various problems are encountered. Because the circuit of Fig. 1 uses a constant current circuit with less temperature dependency and a comparator for comparison with the output voltage Vout, a relatively large amount of circuitry is required for the thermal sensor. Further, it is necessary to minimize the temperature dependency of the operational amplifiers 92 and 94, as well as a reference voltage source Vref. Otherwise, an error arising from the large temperature dependency of each of these components will adversely influence the detected temperature. To remove the adverse influence, most of the circuitry except the bipolar transistor 91 is fabricated and contained in a separate package which is placed at a location such that it is not influenced by the temperature of the power IC. Accordingly, when fabricating the overheating detection circuit in a power IC package, it is necessary to solve the problems associated with the substrate temperature and the increased size of the circuit.

The conventional thermal sensor provides an output signal which varies linearly over a broad range of temperature changes. To the contrary, the conventional overheating detection circuit is designed such that when the temperature of a power device reaches approximately 150°-180° C, it determines that the device temperature has reached an overheating temperature, and produces an output signal. Therefore, the overheating detection circuit must produce an output signal which must vary greatly in accordance with a relatively small temperature range. Thus, the performance requirements of the conventional thermal sensor and overheating detection circuit are quite different from each other.

Accordingly, an object of the present invention is to provide an overheating detection circuit comprising a simple circuit construction which is formed in the same substrate as that of a power device, and which can produce a large output signal in response to a detection of a temperature within a range of detection temperatures. To accomplish the above object, according to a first aspect of the present invention, an overheating detection arrangement for detecting overheating of a power IC is provided which includes a power device integrated in a semiconductor substrate; and an overheating detection circuit comprising: a reverse biased pn junction formed in the same semiconductor substrate as the power device and having a reverse leakage current flow which is temperature dependent; voltage means formed in the same semiconductor substrate as the power device and coupled to the pn junction for produc-

ing a voltage proportional to the reverse leakage current flow; and threshold means connected to the overheating detection circuit for receiving the proportional voltage and producing a signal when the proportional voltage exceeds a threshold voltage to indicate that the power device is overheated.

According to a second aspect of the present invention, the above object can also be achieved by providing an overheating detection arrangement for detecting overheating of a power IC which includes a power device integrated in a semiconductor substrate; and an overheating detection circuit comprising: first and second temperature detecting circuits, the first temperature detecting circuit having a first temperature threshold and the second temperature detecting circuit having a second temperature threshold lower than the first temperature threshold, each of the first and second temperature detecting circuits including: a reverse biased pn junction formed in the same substrate as the power device and having a reverse leakage current flow which is temperature dependent; voltage means formed in the same substrate as the power device and coupled to the pn junction for producing a voltage proportional to the reverse leakage current flow; and threshold means connected to the voltage means for receiving the proportional voltage and producing a signal when the proportional voltage exceeds a threshold voltage corresponding to the respective threshold temperature; and hysteresis means receiving the signals produced by the respective threshold means of the first and second temperature detecting circuits for producing an overheating signal in response to the signal from the threshold means of the first temperature detecting circuit indicating that the power device is overheated and continuing to produce the overheating signal until the signal produced by the threshold means of the second temperature detecting circuit is discontinued.

The voltage means employed in the first and second aspects of the present invention as described above preferably comprises, a depletion type MOSFET (metal oxide semiconductor field effect transistor), a resistance layer, or an enhancement type MOSFET connected to high electric potential.

The reverse leakage current flowing in the reverse biased junction means increases along with an increase in temperature of the substrate where the overheating detection circuit and the power device are formed. The leakage current is converted into a proportional voltage by the voltage means. The converted voltage signal is checked to determine whether it is within the overheating temperature range by using the signal means having a threshold value. When the voltage signal reaches the overheating temperature range, the threshold means, preferably in the form of a comparator having a threshold voltage at one input with the proportional voltage at the other input, produces output (one value of a two-value signal) indicative of overheating. A protective measure against thermal destruction of the power device can then be taken, for example, a load connected to the power IC can be disconnected in accordance with the output of the comparator.

The overheating detection circuit of the present invention is formed with the logic region in the control region of the power IC and is thus in the same substrate as that of the power device. Various techniques are available to prevent a mutual interaction between the control region and the power device, including, for example, a dielectric isolation method utilizing insulation film, a junction isolation method utilizing a pn junction and a self-isolation method utilizing the pn junction of the device itself in which the device is controlled by the gate isolated with the substrate. The self-isolation method is preferred for reasons of economy. The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of embodiments thereof taken in conjunction with the accompanying drawings.

Further advantages of the invention will be apparent from a reading of the following description in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing a conventional overheating detection circuit;

Fig. 2 is a graph showing V_{BE} versus temperature characteristic curves useful for explaining the principle of the conventional overheating detection circuit of Fig. 1;

Fig. 3 is a cross-sectional view of an integrated circuit illustrating the junction structure of a first embodiment of an overheating detection circuit according to a first aspect of the present invention;

Fig. 4 is a cross-sectional view of a power device comprising a metal oxide silicon field effect transistor which is formed in the same semiconducting substrate as that of Fig. 3;

Fig. 5 is a circuit diagram of the first embodiment using the overheating detection circuit shown in Fig. 3;

Fig. 6 is a graphical representation of variations of the reverse leakage current of the pn junction versus voltage at different temperatures, and variations of the current of the MOSFET versus voltage useful in explaining an operation of the circuit shown in Fig. 5;

Fig. 7 is a graphical representation of variations of a doping concentration of the p+ type layer of the pn junction versus error in detected tem-

off in accordance with the output of the comparator.

Fig. 5 is a circuit diagram formed by utilizing the semiconductor structure shown in Fig. 3, and the same components as those in Fig. 3 are indicated by the same reference numerals. The diode 1 consisting of the p+ type region 13 and the n+ type region 16 is connected to the depletion type MOSFET 2 having the n+ type region 17 as source, the n+ type region 18 as drain and the gate electrode 22 in series. The mid-point between the diode 1 and the MOSFET 2 is connected to one input of a comparator 5 which has a threshold voltage V_{th} at its other input.

Next, the operation of the overheating detection circuit shown in Fig. 5 will be described with reference to Fig. 6. In Fig. 6, curve 40 depicts a variation of the current of the MOSFET 2 with respect to the electric potential V_c at the mid point between mode 1 and MOSFET 2. The variation of the current of MOSFET 2 is dependent on the form of MOSFET 2 or the concentration of the n- type region 15. Curves 41, 42, 43, 44, 45 and 46 depict a variation of the reverse leakage current of diode 1 with respect to variations of temperature from T1 to T6. The reverse leakage current varies depending on exp(-1/T), and is increased along with the increase in temperature. Fox example, the reverse leakage current, which is 50×10^{-15} A at 15°C, increases to 200 nA at 175°C. The reverse leakage current also varies depending on the pn junction area. The electric potential V_c is determined by points where the curve 40 intersects the curves 41-46 at the respective temperatures, so that for example the voltage V_c is at V_1 at temperature T1 and varies to V_5 at T5. Comparator 5, having a threshold voltage V_{th}, produces a detecting signal Vout having one value when the electric potential V_c is lower than the threshold voltage V_{th}, and a second value when V_c exceeds the threshold voltage. Therefore, if a control signal derived from the detecting signal Vout is input to the gate electrode of the power device shown in Fig. 4 through a logic circuit (not shown) determining a priority between the control signal and the driving signal of the power device, the power IC can be protected from thermal destruction.

As mentioned above, since the electric potential of the output terminal V_D of the power circuit is changed by the ON-OFF switching of the MOSFET (Fig. 4), errors occur in the detected temperature due to the output voltage potential. That is, the temperature tends to be detected lower than the real temperature when the output voltage is near GND potential by turning ON of the MOSFET. This is caused by the current amplification of the parasitic transistor formed by n+ type region 16, p+ type region 13 and n- type layer 12.

Fig. 7 is a curve showing the development of the error in the detected temperature as a function of concentration of the impurities. As seen, the error in the detected temperature can be suppressed if the parasitic transistor h_{FE} is suppressed by increasing the concentration of p+ type layer 13. Although it depends on the design of the controlling circuit for the power device, a practical overheating detection circuit can be obtained by increasing the concentration of p+ type layer 13, which is on the side of the low impurity concentration layer of the pn junction, to not less than about $5 \times 10^{13}/cm^2$, preferably about $3 \times 10^{14}/cm^2$.

As shown in Fig. 8, the overheating detection circuit according to a second aspect of the present invention comprises a first detecting circuit 61 and a second detecting circuit 62 each having circuit arrangements resembling that of the first aspect of the invention (e.g., Fig. 3), and a hysteresis circuit 63 for receiving output signals V_{11} and V_{12} of the first and second detecting circuits 61 and 62. Diode 1 and FET 2 of detecting circuit 61 and diode 3 and FET 2 of detecting circuit 62 are formed in the same semiconducting substrate as that of the power device shown in Fig. 4. Comparator 5 in each detecting circuit 61, 62 may be integrated in the same substrate if desired. The hysteresis circuit 63 comprises an invertor 51 for inverting the output signal V_{12} of the first detecting circuit 61, and NAND gates 52 and 53 coupled with each other in a feedback manner. The NAND gates 52 and 53 receive the output signal V_{11} of the second detecting circuit 62 as a reset signal, respectively, and output a composite signal V_x and an inverted signal $\bar{v}_x$, respectively. In the circuit arrangement of Fig. 8, a difference of the detecting temperatures between the detecting circuits 61 and 62 is set by properly selecting a junction area of the pn junctions 1 and 3. For instance, if the ratio of the junction area of the diode 1 to that of the diode 3 is 1:4 to 1:5, a temperature difference is produced between the first detecting circuit 61 having the detection temperature of 180°c and the second detecting circuit 62 having the detection temperature of 155°C.

An operation of the overheating detection circuit shown in Fig. 8 will now be described. A threshold voltage of comparator 5 in the first and second detecting circuits 61 and 62, respectively is set to a value corresponding to an overheating detection temperature. The junction area of diode 3 in second detecting circuit 62 is larger than the junction area of diode 1 in first detecting circuit 61 such that detecting temperature T2 of the second detecting circuit 62 is proportionally lower than that of the first detecting circuit 61. The temperature rises, passing through threshold temperature T_2, and reaches the overheating detection temperature

T1 of the first detecting circuit 61. The invertor 51 changes the logic state of its output signal from logic "1" to logic "0". The NAND gates 52 and 53, when receiving the output of invertor 51 at the set terminal, change logical states of the output signals such that the output signal V_x is set to logic "1" and the signal $\bar{v}_x$ is set to logic "0". The changed logic states of the output signals v_x and $\bar{v}_x$ of the NAND gates 52 and 53 are maintained even at the point where the temperature is below the detection temperature within the difference ΔT (T1-T2), and the output signal V_{10} of the invertor 51 changes its logic state. Next, the temperature drops to the detection temperature T2 of the second detector 62. The second detector 62 detects this and changes the logic state of its output signal to logic "1". At this time, the output signal V_x goes low (logic "0"), and the inverted output signal $\bar{v}_x$ goes high. Then, the hysteresis circuit 63 is again placed in the reset state.

As described above, in the overheating detection circuit of Fig. 8, the two temperature detectors 61 and 62 have the two detection temperatures T1 and T2, respectively; and therefore, the preset temperature difference ΔT is provided. The hysteresis circuit 63 performs a hysteresis operation on the basis of the temperature difference ΔT. Therefore, irregular and short period variations in the temperature T of the power device due to a variation of the load at temperatures near the overheating detection temperature, can be ignored as temperature noise. This fact implies that in an overheating state, the power device can be stably held in the off state in accordance with the output signal V_x and the inverted output signal $\bar{v}_x$. With this reference, adverse effects due to unnecessary protection operations on the load circuit, and electromagnetic noise can be reduced. The resultant overheating protection function is reliable.

Fig. 9 is a cross-sectional view showing a semiconducting substrate where the overheating detection circuit according to a first embodiment of the present invention is intended to be formed in the same semiconductor substrate as that of a power device (not shown) comprising an insulated gate field effect transistor (IGBT, IGT or COMFET). In this embodiment, although the p+ type substrate 10 is utilized instead of the n+ type substrate 11 in Fig. 3, the diode consisting of p+ type region 13 and n- type layer 12 as well as the MOSFET consisting of n- type region 15, n+ type region 17, 18 and the gate electrode 22 can be manufactured through the same process steps as in Fig. 3. In addition, the embodiments of the present invention shown in Fig. 3 and Fig. 9 can be applied to a p channel insulated gate type power device with reversed conductive type. In that case, GND is changed to maximum electric potential.

As an alternative to the embodiments in which a depletion type MOSFET is utilized as the voltage conversion means, a resistance or an enhancement type MOSFET may be utilized as the voltage conversion means. In this case, since an n- type layer, n+ type layer or polycrystalline silicon layer are utilized as the resistance, they can be manufactured through similar process steps as in the depletion type MOSFET shown in Fig. 3.

Fig. 10 and Fig. 11 are cross-sectional views showing a semiconducting substrate where the overheating detection circuit according to another embodiment of the present invention is formed in the same semiconductor substrate as that of the MOSFET shown in Fig. 4.

Fig. 10 is a second embodiment of the first aspect of the invention where a diffusion resistance layer is utilized as the voltage means of the present invention. The overheating detection circuit according to the embodiment is formed in the same semiconducting substrate as that of the power device as shown in Fig. 4. Figure 10, p+ type diffused region 13, p- type diffused region 14, n- or n+ type diffused resistance region 121 and n+ diffused region 16 are formed in a surface of an n- type epitaxial layer 12 formed on an n+ type substrate 11. Insulating films 25, 26, 27, 28 and 29 are a protective film for exposed junctions on the surface of the substrate and provide insulation between the diffused regions. An electrode 31 connected to GND terminal contacts the p+ type diffused region 13 through a contacting hold 31A. The electrode 31 is electrically connected to the p-type diffused region 14 through the p+ type diffused region 13. An electrode 32 forms a connection between the n+ type diffused area 16, the diffused resistance region 121 and a Vc terminal and an electrode 33 forms a connection between diffused resistance region 121 and a Vdd terminal. These electrodes 31, 32 and 33 are made of metal. A metallic drain electrode 34 contacts the n+ type substrate 11 and is connected to an output terminal Vd on the opposite side of substrate 11.

Fig. 11 is a third embodiment of the first aspect of the present invention where a polycrystalline silicon resistance layer is utilized as the voltage means of the present invention. This third embodiment mainly differs from the second embodiment shown in Fig. 10 in that the polycrystalline silicon resistance layer 122 contacting electrodes 32 and 33 is provided on p- diffusion region 14 through an insulating film 280 instead of the diffusion resistance layer 121 in Fig. 10. In Fig. 10 and Fig. 11, a pn junction consisting of the p+ diffusion region 13 and n+ diffusion region 16 is equivalent to the reversely biased pn junction of the present invention.

Fig. 12 is a circuit diagram formed by utilizing

the integrated circuit construction shown in Fig. 10 and Fig. 11, and the same components as those in Fig. 10 and Fig. 11, are indicated by the same reference numerals. The diode 1 consisting of the p+ type region 13 and the n+ type region 16 is connected to the resistance layers 121, 122 having the electrode 32 at one end and the electrode 33 at another end in series. The mid-point between the diode and the resistance layer is connected to comparator 5 which may be implemented, for example, by a field effect transistor in a known manner.

Fig. 13 is a cross section of an integrated circuit which shows a fourth embodiment of the first aspect of the invention wherein an enhancement type MOSFET is utilized as the voltage means of the present invention. The overheating detection circuit according to this embodiment is formed in the same semiconducting substrate as that of the power device shown in Fig. 4.

Fig. 14 is a circuit schematic of the integrated circuit of Fig. 13 and corresponds to the circuit of Fig. 3 wherein a p+ type diffused region 13, a p- type diffused region 14 and n+ diffused region 16, 17 and 18 are formed in a surface of an n- type epitaxial layer 12 on an n+ type substrate 11. A gate electrode 22 is formed on the surface between the n+ type diffused regions 17 and 18 through an insulating film 21 of polycrystalline silicon. Insulating films 25, 26, 27, 28 and 29 form a protective film for exposed junctions on the surface of the substrate and provide insulation between the diffused regions. An electrode 31 connected to GND terminal contacts the p+ type diffused region 13 through a contacting hole 31A. The electrode 31 is electrically connected to the p- type diffused region 14 through the p+ type diffused region 13. An electrode 32 forms a connection between the n+ type diffused areas 16 and 17 and a Vc terminal, and an electrode 33 forms a connection between the n+ diffused region 18, the gate electrode 22 and a Vdd terminal. These electrodes 31, 32 and 33 are made of metal. A metallic drain electrode 34 contact the n+ type substrate 11 and is connected to an output terminal V_D on the opposite side of substrate 11. The junction means of the present invention is constituted of the p+ type region 13 and the n+ type region 16 and the enhancement type MOSFET as the voltage means of the present invention is constituted by the n+ type diffusion regions 17, 18 and electrode 22.

As mentioned above, the resistance or the enhancement type MOSFET shown in Fig. 10, Fig. 11 and Fig. 13 can be utilized as the voltage means instead of the depletion type MOSFET shown in Fig. 3. Although, by increasing the impurity concentration to not less than about $5 \times 10^{13}/cm^2$, preferably $3 \times 10^{14}/cm^2$, on the side of the low impurity concentration layer in the pn junction, the errors in the detected temperature can be suppressed while the power device is turning ON, there is a disadvantage in that any variation in voltage Vdd will cause the detected temperature to include errors. However, there are some advantages over the first embodiment from the view point of lower cost in that, for example, the process for accumulating a polycrystalline silicon to form the gate electrode 22 is omitted according to the second embodiment shown in Fig. 10 and the process for forming on n-type diffusion layer is omitted according to the third and forth embodiments shown in Fig. 11 and Fig. 13, respectively. The embodiments are thus selected depending on the purpose.

As seen from the foregoing description, in an overheating detection circuit according to the present invention, a reverse leakage current of a reversely biased pn junction is converted into a potential drop proportional to the reverse leakage current by a voltage means. The potential drop is converted into a corresponding 2-value signal by the threshold means such as a comparator with a threshold value. The overheating detection circuit thus described is formed in a substrate in which a power device is also formed. By utilizing a larger temperature dependency of the reverse leakage current of the pn junction diode and the static characteristics of a depletion type MOSFET, a signal corresponding to a temperature change of the power device can be converted into a large voltage change. Therefore, a temperature detection of the overheating detection circuit is very sensitive particularly in the temperature range of 150°C - 180°C. In addition, since the overheating detection circuit and the power device are formed in the same substrate in the same step, a small, inexpensive power IC including an overheating detection circuit is provided.

In a further aspect of the invention, there is provided an overheating detection circuit comprising two detectors, each having a distinct detection temperature and a hysteresis circuit. Irregular and short period variations in the temperature of the power device due to a variation of the load at a temperature near the overheating detection temperature can be ignored as temperature noise if the temperature difference ΔT between the different detection temperatures is appropriately selected. Therefore, adverse effects due to unnecessary repetition of the protection operation, as well as electromagnetic noise caused by it can be eliminated. When an overheating temperature of a power device is detected, the operation of the power device is stopped and its restart is prohibited until it is confirmed that the overheating temperature drops to a temperature in a safety region which is below

the lower end of the ΔT temperature range. Therefore, there is provided an overheating protection circuit which is stably, reliably, and safely operable.

In addition, by increasing the impurity concentration to not less than about $5 \times 10^{13}/cm^2$ on the side of the low impurity concentration layer in the pn junction, the errors for the detected temperature can be suppressed while the power device is turning ON.

It will be understood that the above description of the present invention is susceptible to various modifications, changes and adaptations, and the same are intended to be comprehended within the meaning and range of equivalents of the appended claims.

The present invention has been described in detail with respect to preferred embodiments, and it will now be apparent from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the invention, therefore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

Claims

1. An overheating detection arrangement for detecting overheating of a power integrated circuit, characterized by including:

   a power device integrated in a semiconductor substrate; and

   an overheating detection circuit, including:

   a reverse biased pn junction formed in the same semiconductor substrate as said power device and having a reverse leakage current flow which is temperature dependent;

   voltage means formed in said semiconductor substrate as said power device and coupled to said pn junction for producing a voltage proportional to the reverse leakage current flow; and

   threshold means connected for receiving the proportional voltage and producing a signal when the proportional voltage exceeds a threshold voltage to indicate that said power device is overheated.

2. The arrangement as claimed in claim 1, characterized in that said semiconductor substrate includes a low impurity concentration layer on one side of said pn junction which has an impurity concentration of not less than $5 \times 10^{13}/cm^2$.

3. The arrangement as claimed in claim 1, characterized in that said voltage means comprises a depletion-type MOSFET connected for receiving a constant current.

4. The arrangement as claimed in claim 1, characterized in that said voltage means comprises a diffusion resistance layer.

5. The arrangement as claimed in claim 1, characterized in that said voltage means comprises a polycrystalline silicon resistance layer.

6. The arrangement as claimed in claim 1, characterized in that said voltage means comprises an enhancement-type MOSFET.

7. An overheating detection arrangement for detecting overheating of a power integrated circuit, characterized by including:

   a power device integrated in a semiconductor substrate; and

   an overheating detection circuit comprising:

   first and second temperature detecting circuits, said first temperature detecting circuit having a first temperature threshold and said second temperature detecting circuit having a second temperature threshold lower than the first temperature threshold, each of said first and second temperature detecting circuits including:

   a reverse biased pn junction formed in the same semiconductor substrate as said power device and having a reverse leakage current flow which is temperature dependent;

   voltage means formed in the same semiconductor substrate as said power device and coupled to said pn junction for producing a voltage proportional to the reverse leakage current flow; and

   threshold means connected to said voltage means for receiving the proportional voltage and producing a signal when the proportional voltage exceeds a threshold voltage corresponding to the respective threshold temperature; and

   hysteresis means receiving the signals produced by the respective threshold means of said first and second temperature detecting circuits for producing an overheating signal in response to the signal from the threshold means of said first temperature detecting circuit indicating that said power device is overheated and continuing to produce the overheating signal until the signal from the threshold means of said second temperature detecting circuit is discontinued.

8. The arrangement as claimed in claim 7, characterized in that said semiconductor sub-

strate includes a low impurity concentration layer on one side of each said pn junction which has an impurity concentration of not less than $5 \times 10^{13}/cm^2$.

9. The arrangement as claimed in claim 7, characterized in that each said voltage means comprises a depletion-type MOSFET connected for receiving a constant current.

10. The arrangement as claimed in claim 7, characterized in that each said voltage means comprises a diffusion resistance layer.

11. The arrangement as claimed in claim 7, characterized in that each said voltage means comprises a polycrystalline silicon resistance layer.

12. The arrangement as claimed in claim 7, characterized in that each said voltage means comprises an enhancement-type MOSFET.

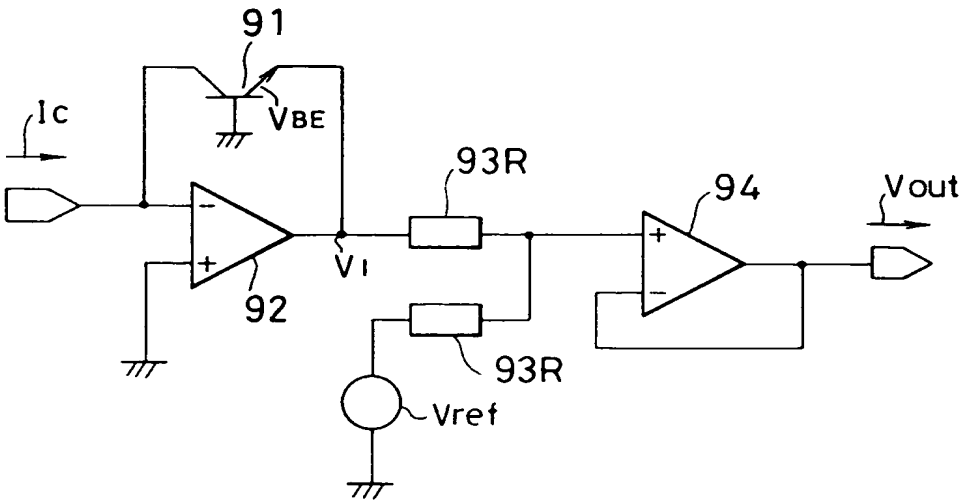


FIG. 1 (PRIOR ART)

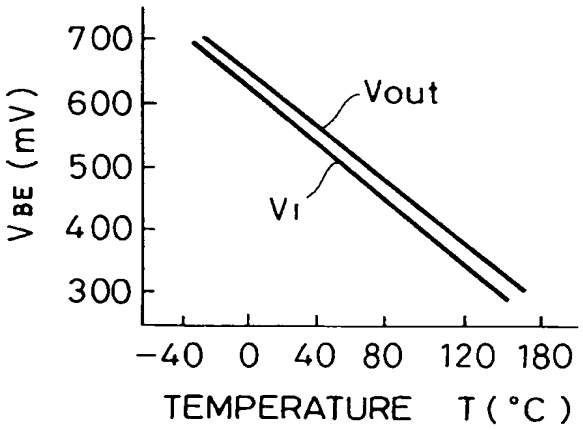
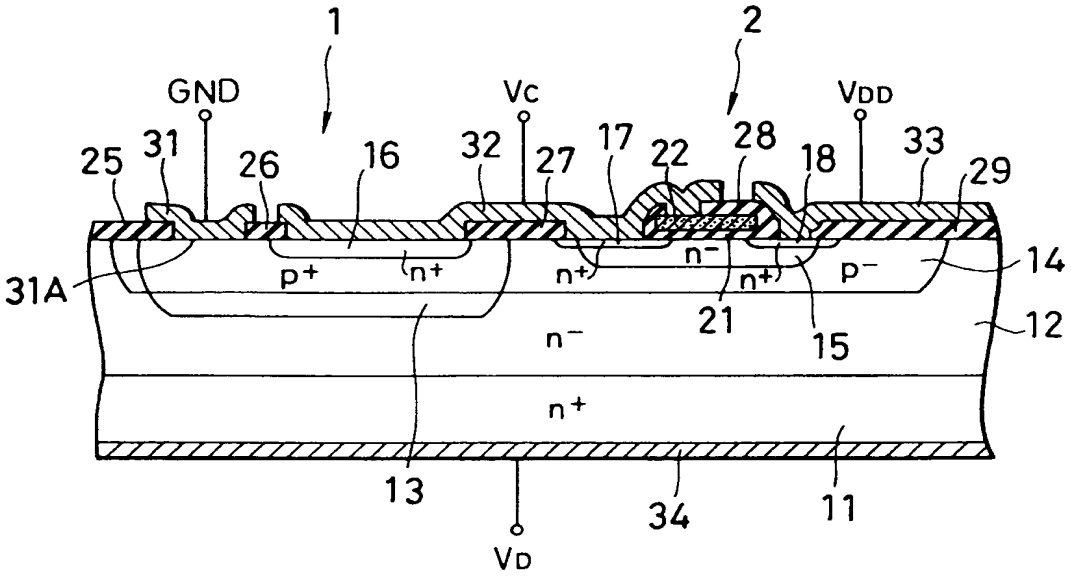


FIG. 2 (PRIOR ART)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12
n−
n+
13
34
11
VD

FIG.3

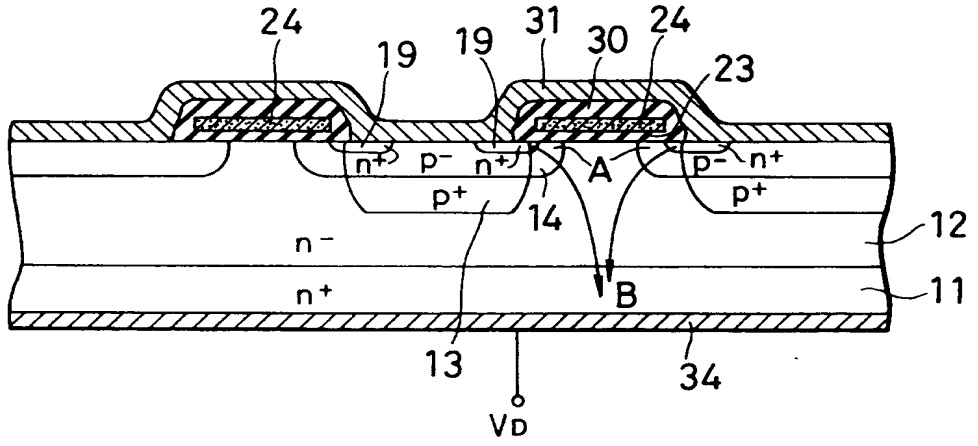
24
19
19
31
30
24
23
n+
p−
n+
A
p−
n+
p+
p+
14
12
n−
n+
B
11
13
34
VD

FIG.4

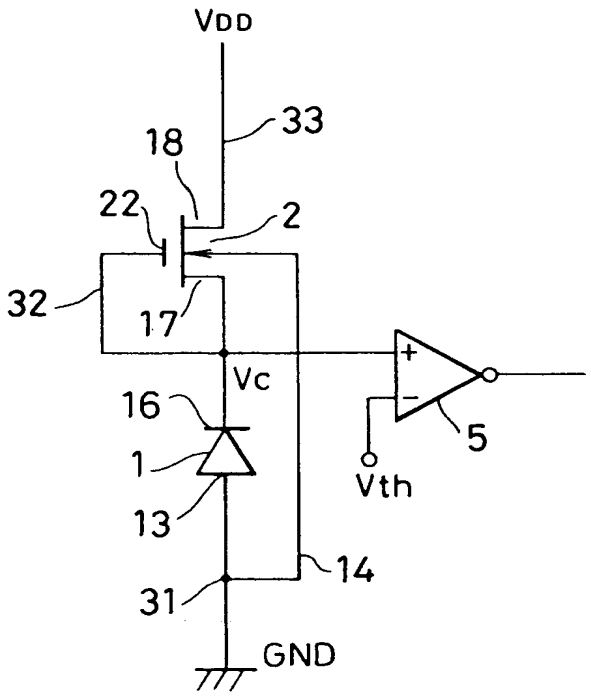

FIG.5

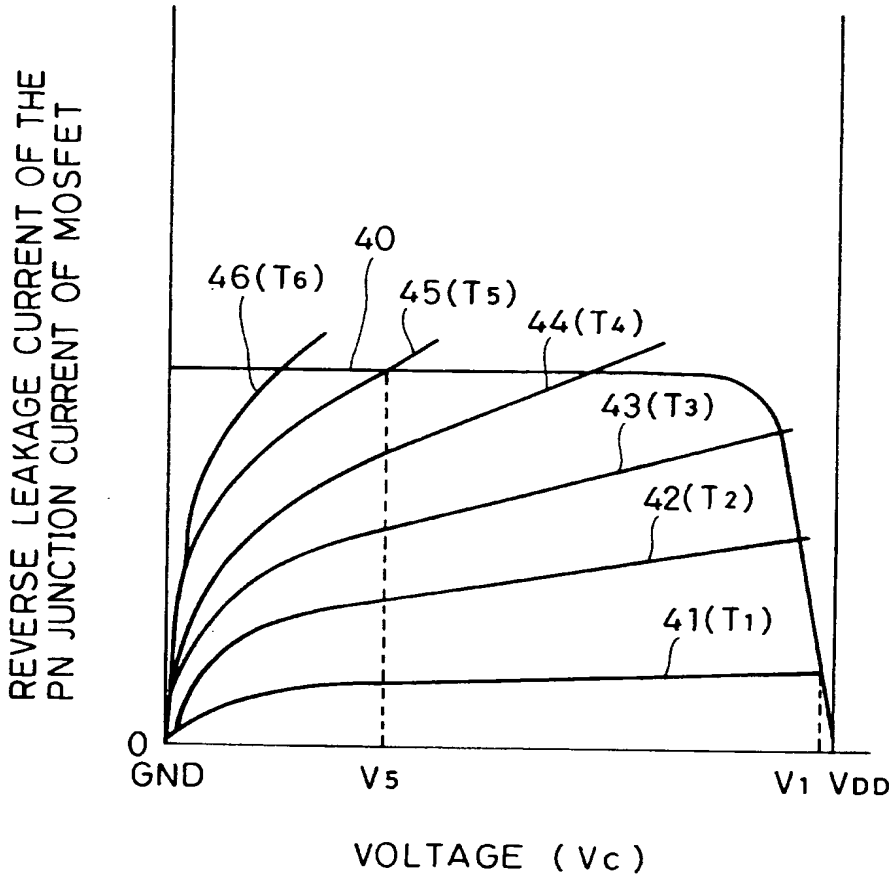
REVERSE LEAKAGE CURRENT OF THE PN JUNCTION CURRENT OF MOSFET
40
46(T6)
45(T5)
44(T4)
43(T3)
42(T2)
41(T1)
0
GND
V5
V1 VDD
VOLTAGE (Vc)

FIG.6

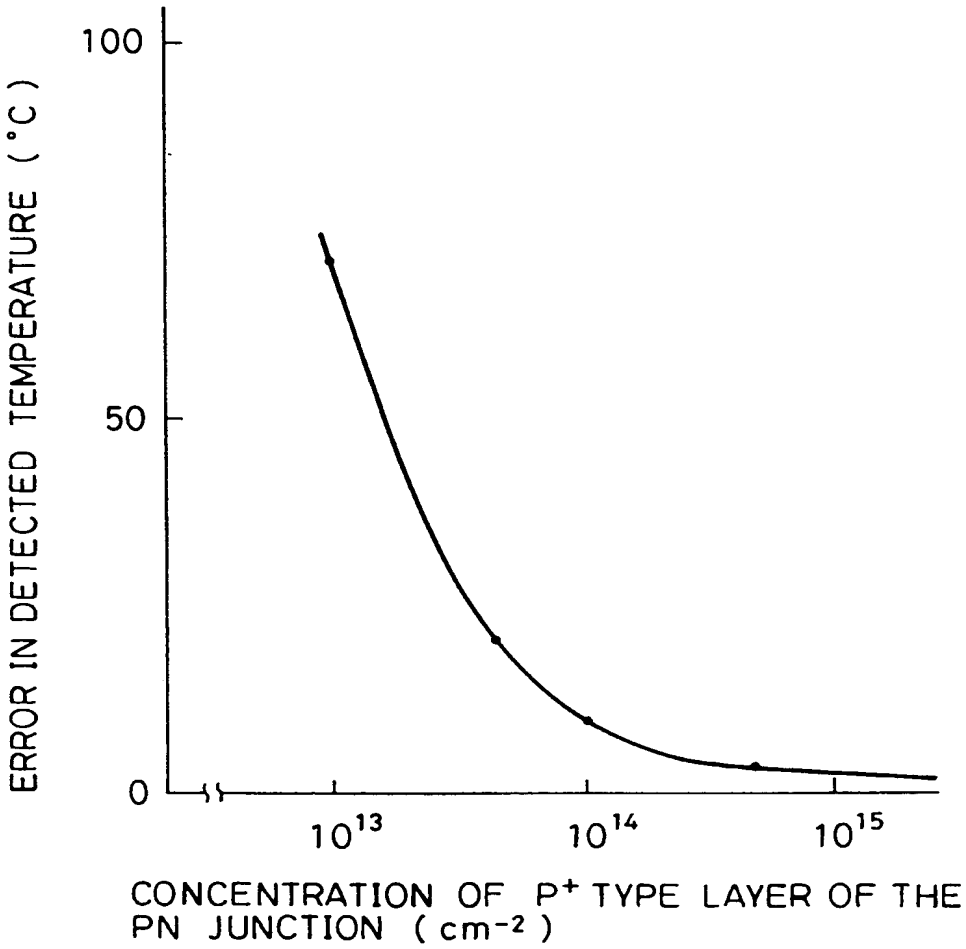
100
50
0
ERROR IN DETECTED TEMPERATURE (°C)
10^{13}
10^{14}
10^{15}
CONCENTRATION OF P^+ TYPE LAYER OF THE PN JUNCTION (cm^{-2})

FIG.7

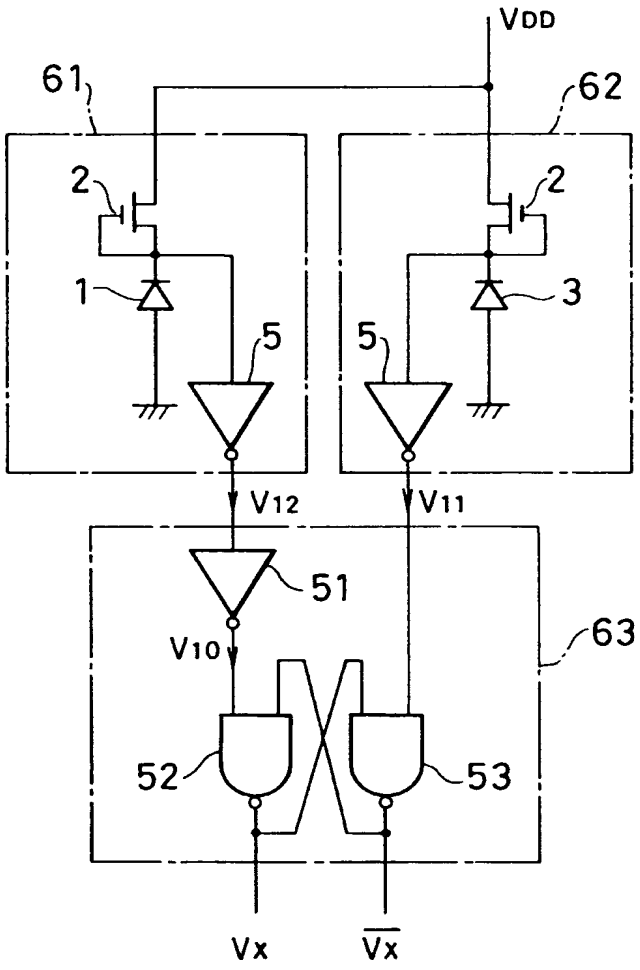

FIG.8

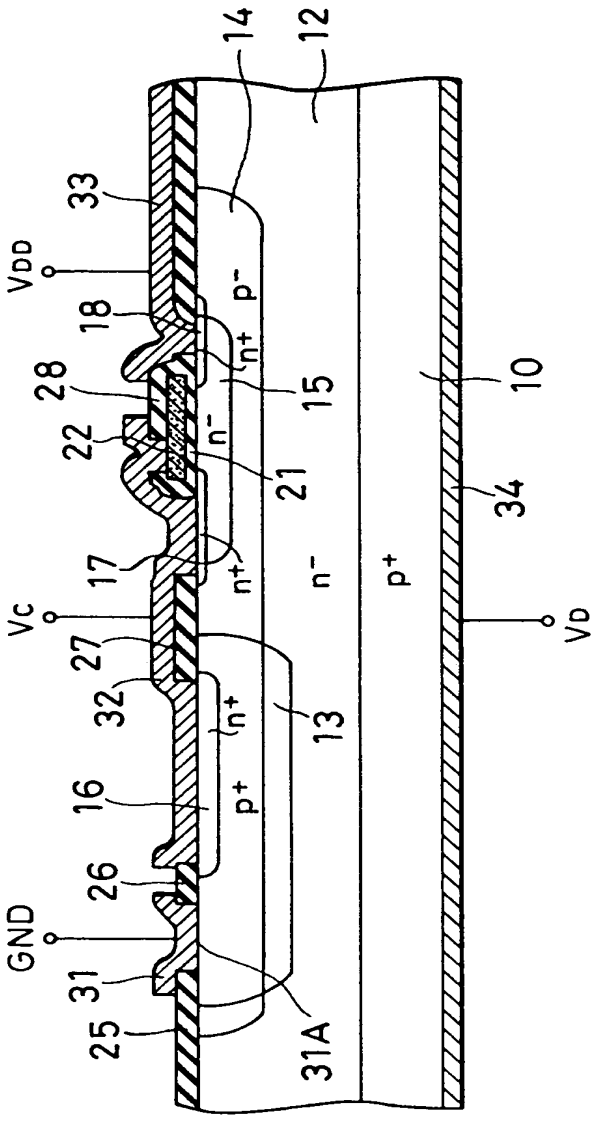
14
12
33
VDD
18
28
22
17
Vc
27
32
16
26
GND
31
25
31A
13
21
15
10
34
VD
p-
n+
n-
p+

FIG.9

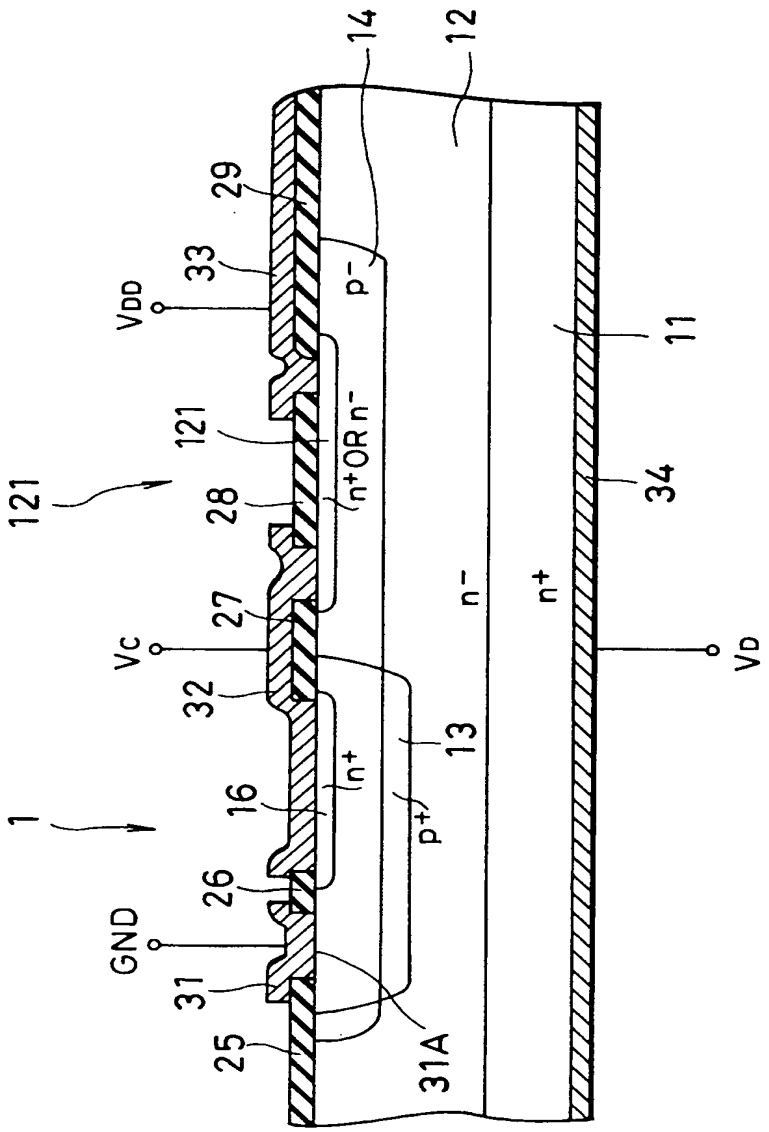
14
12
29
33
VDD
p⁻
11
121
n⁺OR n⁻
121
28
34
27
n⁻
n⁺
VC
VD
32
13
n⁺
1
16
p⁺
26
GND
31
25
31A

FIG.10

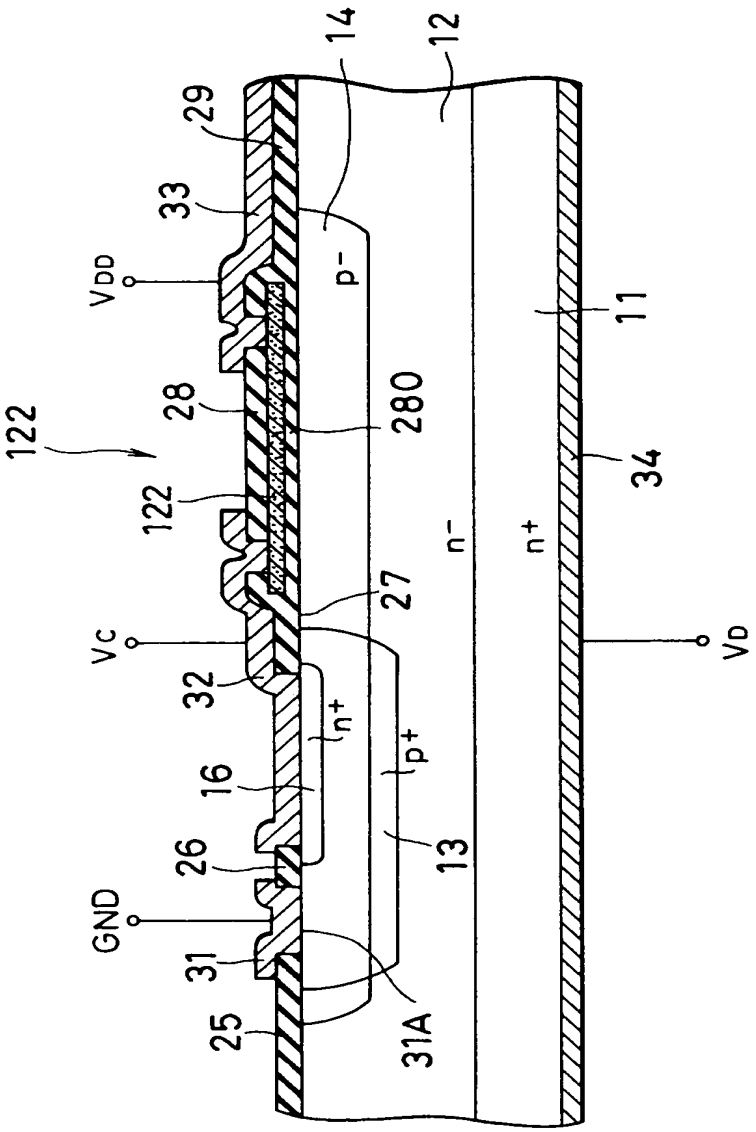
14
12
29
33
VDD
p-
11
122
28
280
34
122
n-
n+
27
Vc
32
VD
n+
p+
16
26
13
GND
31
25
31A

FIG. 11

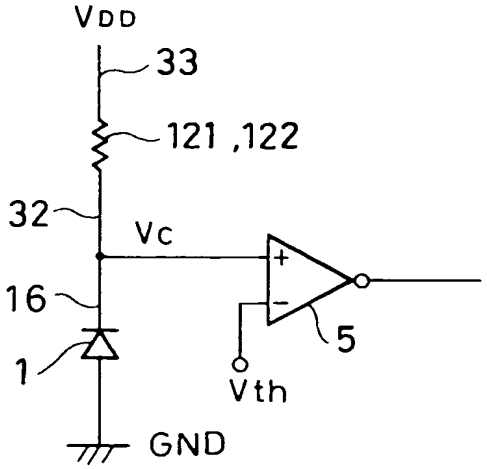
VDD
33
121 ,122
32
Vc
16
1
5
Vth
GND

FIG. 12

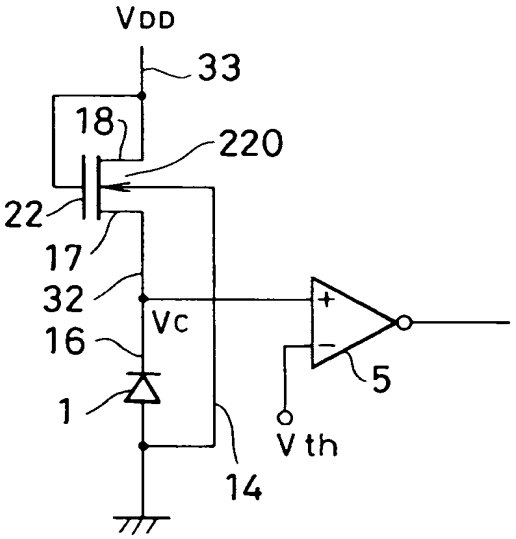
VDD
33
18
220
22
17
32
Vc
16
1
5
Vth
14

FIG. 14

14 12

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 11 9989

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	EP-A-0 409 214 (FUJI ELECTRIC CO) 23 January 1991 * the whole document *	1,7	G01K7/00 G01K3/00
A	DE-A-3 821 460 (MITSUBISHI) * column 17, line 20 - column 19, line 11; figures 16,19 *	1	
A	US-A-4 667 265 (NATIONAL SEMICONDUCTOR CORP.) * the whole document *	1,7	
A	EP-A-0 306 396 (SGS-THOMSON) * the whole document *	1	
A	EP-A-0 174 686 (PHILIPS) * page 4, line 10 - page 4, line 28 *	2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G01K H02H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 JANUARY 1992	RAMBOER P.

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